Appl. No. 10/734,905
Amdt. dated June 2, 2006
Reply to Office Action of December 2, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of computer aided design comprising:

providing a description of a first logic function using a high-level design language;

synthesizing gates to obtain a first alternative netlist for the first logic function;

performing a technology mapping of the first alternative netlist to obtain a first mapping netlist;

synthesizing gates to obtain a second alternative netlist for the first logic function;

performing a technology mapping of the second alternative netlist to obtain a second mapping netlist;

selecting one of corresponding first alternative ~~mapping~~ netlist or second alternative ~~mapping~~ netlist based on a comparison of the first mapping netlist with the second mapping netlist based on design criteria, wherein the selected one of the corresponding first ~~mapping~~ alternative netlist or second ~~mapping~~ alternative netlist is a selected ~~mapping~~ netlist;

optimizing the selected ~~mapping~~ netlist based on the corresponding mapping netlist; and

performing a technology mapping on the selected ~~mapping~~ netlist after optimizing. ~~, wherein the first mapping netlist comprises digital signal processing blocks.~~

2. (Previously Presented) The method of claim 1 wherein the design criteria includes optimizing for area.

3. (Previously Presented) The method of claim 1 wherein the design criteria includes optimizing for delay.

4. (Previously Presented) The method of claim 1 wherein the first mapping netlist comprises look-up table structures.

5. (Cancelled).

6. (Previously Presented) The method of claim 1 wherein the first alternative netlist comprises logic gates.

7. (Previously Presented) The method of claim 1 wherein the step of performing a technology mapping of the first alternative netlist to obtain a first mapping netlist is done on a copy of the first alternative netlist.

8. (Currently Amended) A method of logic synthesis comprising:

generating a first alternative netlist for a logic function;

generating a second alternative netlist for the logic function, wherein the second alternative netlist has a different gate configuration from the first alternative netlist; and

selecting one of the first alternative netlist or the second alternative netlists as a selected alternative netlist based on results of a technology mapping of the first alternative netlist and the second alternative netlists~~, wherein the first alternative netlist includes a digital signal processing block.~~; and

optimizing the selected netlist based on results of a technology mapping of the first alternative netlist and the second alternative netlists; and

performing a technology mapping on the selected mapping netlist after optimizing.

9. (Previously Presented) The method of claim 8 further comprising:

performing a synthesis optimization on the selected alternative netlist to obtain an optimized selected alternative netlist.

10. (Previously Presented) The method of claim 8 further comprising:

performing a synthesis optimization on the selected alternative netlist to obtain an optimized selected alternative netlist; and

performing a technology mapping on the optimized selected alternative netlist.

11. (Previously Presented) The method of claim 8 wherein the selecting one of the first alternative netlist or the second alternative netlists is based on area.

12. (Previously Presented) The method of claim 8 wherein the selecting one of the first alternative netlist or the second alternative netlists is based on depth.

13. (Currently Amended) A method of logic synthesis comprising:

generating a netlist for a logic function;

performing a first technology mapping on the netlist;

after the first technology mapping, performing a synthesis optimization on the netlist; and

after the synthesis optimization, performing a second technology mapping on the netlist~~, wherein the first technology mapping includes a digital signal processing block~~.

14. (Previously Presented) The method of claim 13 wherein the first technology mapping maps the netlist to the same target technology as the second technology mapping.

15. (Previously Presented) The method of claim 13 wherein the logic function is provided in a high-level design language.

16. (New) The method of claim 1 wherein the first mapping netlist comprises digital signal processing blocks.

17. (New) The method of claim 8 wherein the first alternative netlist comprises digital signal processing blocks.

18. (New) The method of claim 13 wherein the first technology mapping comprises digital signal processing blocks.

19. (New) The method of claim 1, wherein performing the technology mappings of the first and second alternative netlists comprises estimating technology mappings of the first and second alternative netlists to obtain the first and second mapping netlists.

20. (New) The method of claim 13, wherein performing the synthesis optimization on the netlist includes optimizing the netlist based on the results of the first technology mapping.